Chips

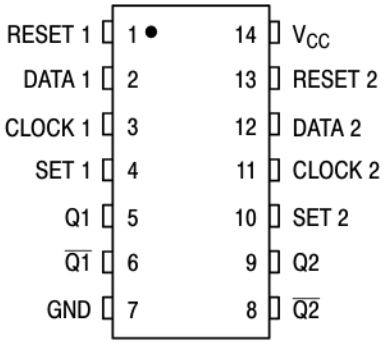
TTL

74HC74 - Dual D Flip?Flop with Set and Reset

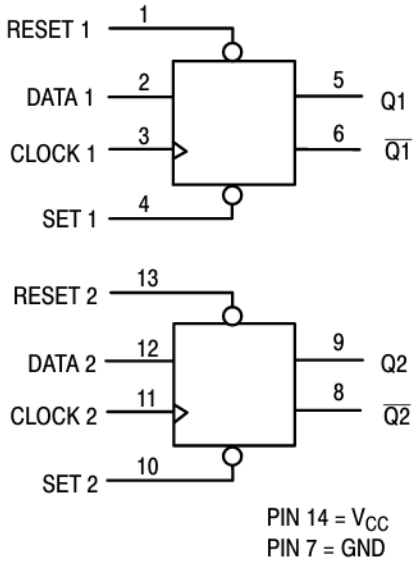
- 74HC74.pdf

74HC74

PIN ASSIGNMENT



LOGIC DIAGRAM



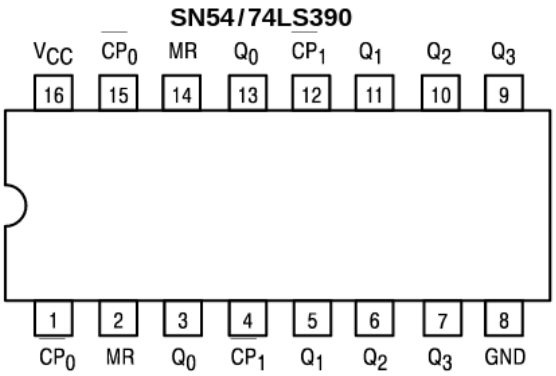
FUNCTION TABLE

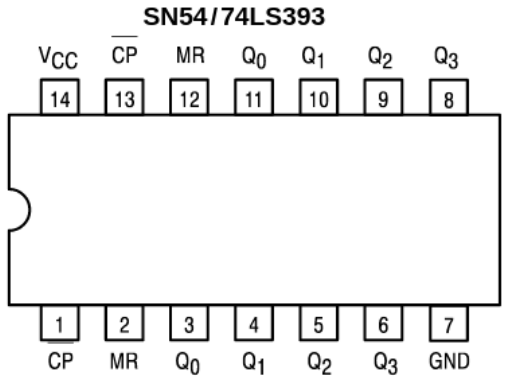
Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

SN54LS393 - Dual 4-Stage Binary Counter

- SN54LS390.PDF





PIN NAMES

$\overline{CP}$	Clock (Active LOW going edge) Input to +16 (LS393)
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 (LS390)
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 (LS390)
MR	Master Reset (Active HIGH) Input
$Q_0 - Q_3$	Flip-Flop outputs (Note b)

SN54/74LS390 BCD TRUTH TABLE
(Input on CP_0; Q_0 CP_1)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

SN54/74LS390 ÷5 TRUTH TABLE
(Input on CP_1)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	
0	L	L	L	
1	L	L	H	
2	L	H	L	
3	L	H	H	
4	H	L	L	

SN54/74LS390 ÷10 (50% @ Q_0) TRUTH TABLE
(Input on CP_1, Q_3 to CP_0)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	H	L
2	L	H	L	L
3	L	H	H	L
4	H	L	L	L
5	L	L	L	H
6	L	L	H	H
7	L	H	L	H
8	L	H	H	H
9	H	L	L	H

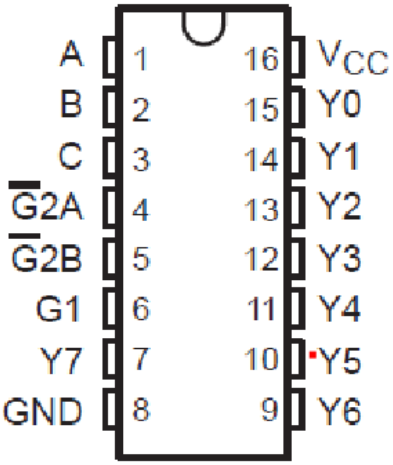
SN54/74LS393 TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

SNx4HCT138 - 3-Line to 8-Line Decoders/Demultiplexers

- sn74hct138.pdf



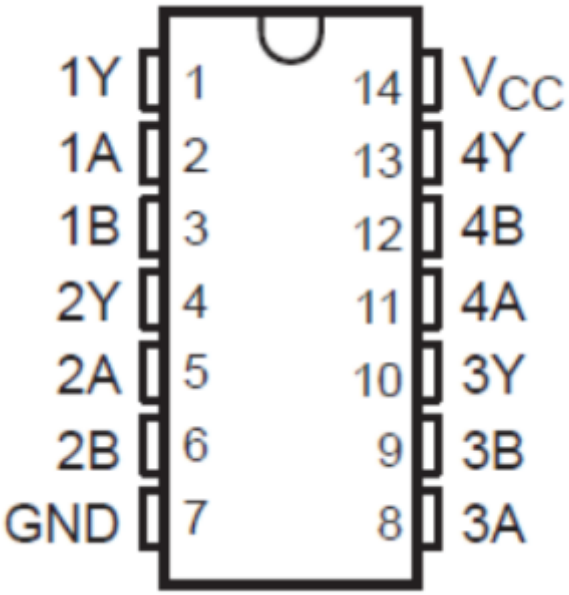
J, W, D, N, NS, or PW Package
16-Pin CDIP, CFP, SOIC, PDIP, SO, TSSOP
Top View

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

SN74HCT02

Contain four independent 2-input NOR gates.

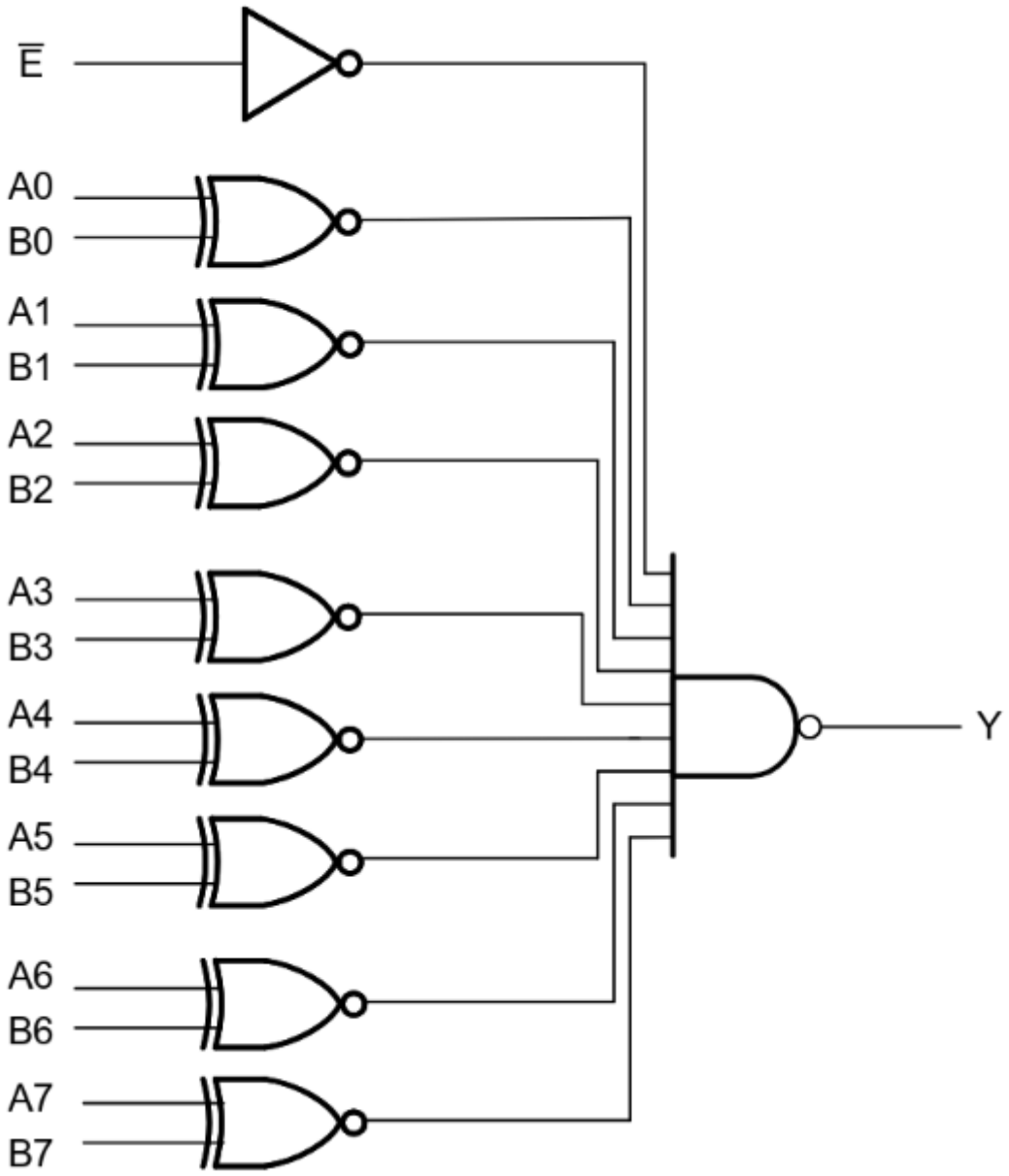
- sn74hct02.pdf

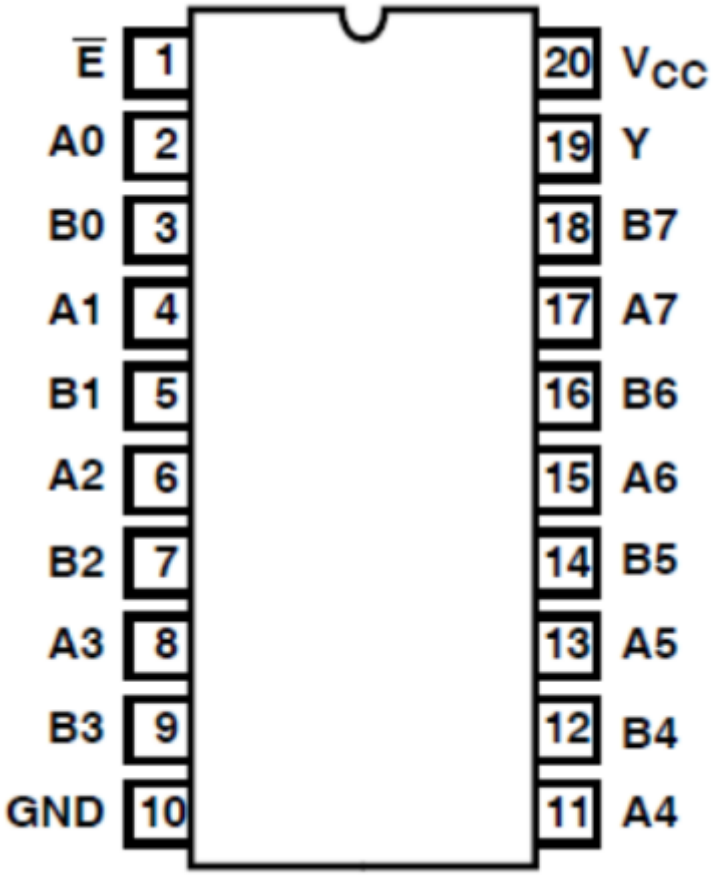


INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

CD74HCT688

8-Bit Magnitude Comparator.


$\overline{E}$
A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
B5
A6
B6
A7
B7
Y

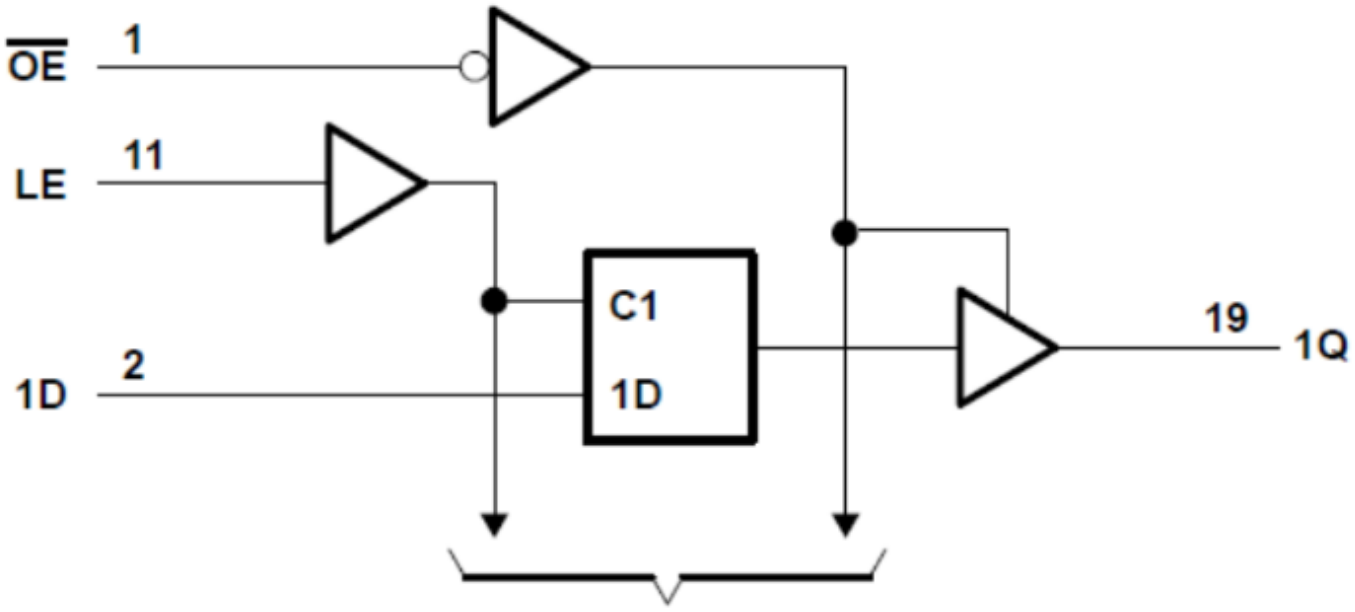


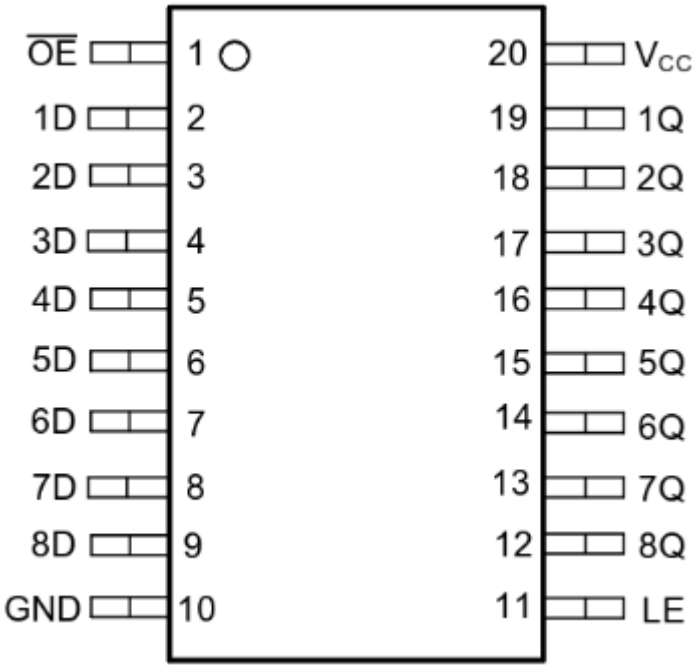
INPUTS		OUPUTS
A, B	$\overline{E}$	Y
A = B	L	L
A ≠ B	L	H
X	H	H

SNx4HCT573

Octal Transparent D-Type Latches With 3-State Outputs.

- sn74hct573.pdf





INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

DS1233

Keeps CPU in reset until VCC stabilizes, also debounces a reset button.

- 5V EconoReset

PIC MCU

PIC16F84

- Intro: The PIC 16x8x Family, PIC16F84: Everything You Should Know
- Datasheet: PIC16x84.pdf
- Programming: PIC16F8X_prog.pdf
- Asm: `xq gputils` https://gputils.sourceforge.io/
- Simulator: `xq gpsim` https://gpsim.sourceforge.net/

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